Amendments to the Claims:

This Listing of Claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-32 (canceled).

Claim 33 (currently amended): A method of designing an integrated circuit comprising:

creating a netlist design for each of a set of sub-circuits, each sub-circuit performing an electronic operation and having at least 300 gates;

creating a physical layout for each such sub-circuit which layout includes information defining the physical position of all components of the sub-circuit, and locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit;

defining desired electrical interconnections among all of the components of the sub-circuit, the electrical connections being defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later;

defining interconnection information for providing electrical connections as needed among such components;

optimizing the design and layout for each such sub-circuit to obtain a desired level of operating speed for such sub-circuit independently of any use of such sub-circuit with any other sub-circuit, to thereby provide a completed design for the sub-circuit;

storing such ~~optimized~~ completed design of the sub-circuit for later use in conjunction with other sub-circuits and other circuits;

creating a netlist design for the integrated circuit which includes at least two sub-circuits previously optimized and stored;

creating a physical layout for the integrated circuit by placing the at least two sub-circuits without changing the completed design of the sub-circuit on a design in proximity to each other; which layout includes information defining the physical position of the at least two

sub-circuits and the locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit; and

defining desired electrical interconnections among the sub-circuits, the electrical connections being defined entirely on layers other than the layers used for the desired electrical interconnections among the components of the sub-circuits.

Claim 34 (previously presented): The method of claim 33 wherein in the step of defining desired electrical interconnections among all of the components of the sub-circuit, the electrical connections being defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later, at least one layer of the electrical interconnections does not include both power and clock signals.

Claim 35 (previously presented): The method of claim 33 wherein the plurality of layers are each layers having electrically conductive material thereon, with vias between at least two adjoining layers.

Claim 36 (currently amended): The method of claim 33 wherein as a result of the step of storing such completed design, each sub-circuit has a predefined size and shape, and that size and shape are not changed by the step of creating a netlist design for the integrated circuit which includes at least two sub-circuits previously optimized and stored.

Claim 37 (previously presented): The method of claim 33 wherein each sub-circuits has predefined interconnection locations for connecting that sub-circuit to at least one other sub-circuit.

Claim 38 (previously presented): The method of claim 37 wherein each sub-circuit provides one of a plurality of logic functions.

Claim 39 (previously presented): The method of claim 38 wherein at least two sub-circuits having different size and shape provide the same logic function.

Claim 40 (previously presented): The method of claim 33 wherein each sub-circuit comprises a physical representation of a logic circuit.

Claim 41 (previously presented): The method of claim 40 wherein each sub-circuit is defined by at least one GDSIII file.

Claim 42 (previously presented): The method of claim 33 wherein each sub-circuit comprises on the order of 1000 gates.

Claim 43 (previously presented): The method of claim 33 wherein no layer in the layers available for the provision of interconnections in an integrated circuit to be designed later includes both electrical connections for interconnecting components of the sub-circuit and electrical connections for connecting one sub-circuit to another.

Claims 44-64 (canceled).

Claim 65 (new): A method of designing an integrated circuit which includes at least two predefined sub-circuits, the method comprising:

creating a netlist design for each of the at least two sub-circuits, each sub-circuit performing an electronic operation and having at least 300 gates;

creating a physical layout for each such sub-circuit which layout includes information defining the physical position of all components of the sub-circuit, and locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit;

defining desired electrical interconnections among the components of the sub-circuit, the electrical connections being defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later;

improving the design for each such sub-circuit to obtain a desired level of operating speed for such sub-circuit independently of any use of such sub-circuit with any other sub-circuit to thereby define for each such sub-circuit a configuration having a shape;

for each such sub-circuit, storing such improved design and shape for later use in conjunction with other sub-circuits;

creating a netlist design for the integrated circuit which integrated circuit includes the at least two sub-circuits previously stored;

creating a physical layout for the integrated circuit by placing the at least two sub-circuits in proximity to each other; which layout includes information defining the physical position of the at least two sub-circuits on the integrated circuit; and

defining desired electrical interconnections among the sub-circuits, the electrical connections being defined entirely on layers other than the layers used for the desired electrical interconnections among the components of the sub-circuits.

Claim 66 (new): The method of claim 65 wherein in the step of defining desired electrical interconnections among all of the components of the sub-circuit, the electrical connections being defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later, at least one layer of the electrical interconnections does not include both power and clock signals.

Claim 67 (new): The method of claim 65 wherein each sub-circuit provides one of a plurality of logic functions.

Claim 68 (new): The method of claim 67 wherein at least two sub-circuits having different size and shape provide the same logic function.

Claim 69 (new): The method of claim 65 wherein each sub-circuit comprises a physical representation of a logic circuit.

Claim 70 (new): The method of claim 69 wherein each sub-circuit is defined by at least one GDSIII file.

Claim 71 (new): The method of claim 65 wherein each sub-circuit comprises on the order of 1000 gates.

Claim 72 (new): The method of claim 65 wherein no layer in the layers available for the provision of interconnections in an integrated circuit to be designed later includes both

electrical connections for interconnecting components of the sub-circuit and electrical connections for connecting one sub-circuit to another.